What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of patterning a metal, said method comprising the steps of:

placing a surface of said metal in fluid communication with a second surface by placing said metal and said second surface in a fluid bath;

supplying a current to the metal surface and said second surface; and

moving at least one of the surfaces relative to the other.

2. The method of claim 1, wherein the metal comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

3. The method of claim 1, wherein the metal comprise platinum.

4. The method of claim 1, wherein the metal has a thickness of less than approximately 1000 angstroms.

5. The method of claim 1, wherein the fluid comprises an acid.

6. The method of claim 1, wherein the fluid comprises hydrochloric acid, water, and potassium chloride.

7. The method of claim 1, wherein the fluid comprises at least one abrasive particle selected from the group consisting of cerium oxide (CeO_2), silicon oxide (SiOx), and aluminum oxide.

8. The method of claim 1, wherein the second surface comprises a conductive material.

9. The method of claim 8 wherein the second surface comprises a conductive polymer.

10. The method of claim 8 wherein the second surface comprises a conductive oxide.

11. The method of claim 8 wherein the second surface comprises a polymer containing conductive particles.

12. The method of claim 1, wherein the second surface comprises at least one polishing surface containing abrasive materials.

13. The method of claim 9, wherein said fixed abrasive particle comprises at least one abrasive particle selected from the group consisting of cerium oxide (CeO_2), silicon oxide (SiOx), and aluminum oxide.

14. The method of claim 1 further comprising providing a working electrode in said fluid bath.

15. The method of claim 1 wherein said second surface comprises a pad.

16. The method of claim 15 wherein said pad contains abrasive materials.

17. The method of claim 1, wherein said current supplying step is performed by applying a pulsed current to the metal surface and said second surface.

18. The method of claim 11, wherein said current is supplied for approximately 200 seconds or less.

19. The method of claim 1, wherein said current supplying step is performed by applying a constant current to the metal surface and said second surface.

20. The method of claim 1, wherein a force is applied to said surfaces, at least one of which is moving relative to the other.

21. A method of patterning at least one metal of a semiconductor device, said method comprising the steps of:

placing a surface of said metal in fluid communication with a second surface by placing said metal and said second surface in a fluid bath;

supplying a current to the metal surface and said second surface; and

moving at least one of the surfaces relative to the other.

22. The method of claim 21, wherein the metal comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

23. The method of claim 21, wherein the semiconductor devices comprises at least one device from the group consisting of capacitor, transistor, resistor, conductor layer, conductive plug, metalization layer, gate metal, interconnect, electrode, electrical contact, electrical via, and bonding pad.

24. A method of patterning at least one metal of a memory element of a semiconductor device, said method comprising the steps of:

placing a surface of said metal in fluid communication with a second surface by placing said metal and said second surface in a fluid bath;

supplying a current to the metal surface and said second surface; and

moving at least one of the surfaces relative to the other.

25. The method of claim 24, wherein the metal comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals metal, and refractory metal alloys.

26. A method of patterning a capacitor electrode of a DRAM memory device, said method comprising the steps of:

placing a surface of the electrode in fluid communication with a second surface by placing said electrode surface and said second surface in a fluid bath;

supplying a current to said electrode surface and said second surface; and

moving at least one of the surfaces relative to the other.

27. The method of claim 26 wherein said electrode comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals metal, and refractory metal alloys.

28. The method of claim 26, wherein said electrode comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals metal, and refractory metal alloys.

29. A method of forming a semiconductor device, comprising the steps of:

forming a conductive layer over an insulating layer;

forming a metal layer over said conductive layer;

forming a protective layer over portions of said metal layer, leaving other portions of said metal layer exposed; and

electro-mechanical polishing said exposed portions of said metal layer.

30. The method of claim 29, wherein said metal layer comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

31. The method of claim 29, wherein said protective layer comprises a photoresist material.

32. The method of claim 29 wherein said protective layer comprises a spin on glass.

33. The method of claim 29, further comprising the step of forming an opening into said insulating layer, said conductive layer, metal layer, said protective layer being formed in said opening.

34. The method of claim 29, wherein said metal layer forms a bottom capacitor electrode of said semiconductor device.

35. A method of forming a capacitor electrode, said method comprising the steps of:

forming an electrode by depositing a metal in a container structure in electrical communication with a conductive layer;

covering an exposed surface of the metal inside said container with a protective material;

placing the exposed surface of the metal in fluid communication with a second surface by placing the exposed metal surface and said second surface in a fluid bath;

supplying a current to the metal surface and said second surface; and

moving at least one of the surfaces relative to the other.

36. The method of claim 35, wherein said capacitor electrode is a bottom electrode.

37. A method of forming a lower electrode of a capacitor on a semiconductor substrate, comprising the steps of:

forming a first opening into a first insulating layer provided over said semiconductor substrate;

forming a conductive plug in said first opening;

forming a second insulating layer over said conductive plug and said first insulating layer;

forming a second opening into said second insulating layer over said conductive plug;

forming a metal layer in said opening and over at least a portion of said second insulating layer;

forming a protective layer over portions of said metal layer, leaving other portions of said metal layer exposed; and

electro-mechanical polishing said exposed portions of said metal layer.

38. The method of claim 37, wherein said electrode comprises at least one metal from the group consisting of noble metals, noble metal alloys, refractory metals metal, and refractory metal alloys.

39. A semiconductor device comprising:

a substrate; and

at least one electro-mechanical polished metal layer formed over said substrate.

40. The semiconductor device of claim 39, wherein said metal layer comprises at least one metal selected from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

41. The semiconductor device of claim 39, wherein said device comprises a capacitor with at least one electro-mechanical polished metal layer.

42. The semiconductor device of claim 41, wherein said electro-mechanical polished metal layer is a bottom electrode of said capacitor.

43. A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an mechanical-electro polished surface.

44. The capacitor of claim 43, wherein said capacitor is a MIM capacitor.

45. The capacitor of claim 43, wherein at least one electrode comprises a metal selected from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

46. The capacitor of claim 43, wherein said at least one electrode surface is a surface of said bottom electrode.

47. The capacitor of claim 38, wherein the bottom electrode comprises a platinum electrode.

48. A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising

a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished layer provided over said substrate.